What Is Claimed Is:

1. A package board having a core board on each surface of which a plurality of conductor circuits are formed with an interlaminar resin insulating layer therebetween, wherein a plurality of soldering pads are formed on the IC chip mounted side surface, as well as on the other side surface to be connected to another board, so that said soldering pads on the other side surface are larger than those on said IC chip side surface of said package board, and

a dummy pattern is formed between conductor circuit patterns formed on said IC chip mounted side surface of said core board.

2. A package board having a core board on each surface of which a plurality of conductor circuits are formed with an interlaminar resin insulating layer therebetween, wherein a plurality of soldering pads are formed on the IC chip side surface, as well as on the other side surface to be connected to another board, so that said soldering pads on the other side surface are larger than those on said IC chip side surface of said package board, and

a dummy pattern is formed at the outer periphery of each conductor circuit formed on said IC chip side of said core board.

3. A package board composed as a multi-layer wiring board, comprising:

a plurality of conductor circuits formed in an outermost layer;

an insulating layer for supporting a plurality of said conductor circuits formed in said outermost layer; and

a plurality of inner layer conductor circuits formed under said insulating layer, wherein

a plurality of said inner layer conductor circuits are a power supply layer and/or a ground layer,

a soldering bump is formed, through said insulating layer, on each via-hole connected to an inner layer conductor circuit.

4. A package board composed as a multi-layer printed wiring board, comprising:

first conductor circuit formed in an inner layer;

first interlaminar resin insulating layer formed on said first inner layer conductor circuit;

second inner layer conductor circuit formed on said first interlaminar resin insulating layer;

second interlaminar resin insulating layer formed on said second conductor circuit; and

a plurality of conductor circuits formed in the outermost layer formed on said second interlaminar resin insulating layer, wherein

a plurality of said second conductor circuits in said inner layer is a power supply layer and/or a ground layer, and

a soldering bump is formed, through said second interlaminar resin insulating layer, in each via-hole connected to a second conductor circuit.

5. A package board having a core board with a conductor layer formed on each surface, another conductor layer formed on said conductor layer with an interlaminar resin insulating layer therebetween, and a conductor layer on either of said surfaces of said core board being used as an electrode layer, wherein

the land of a through-hole of said core board, disposed in a conductor layer formed as said electrode layer, is united with a pad connected to a via-hole formed through an interlaminar resin insulating layer formed on the top surface of said package board.

6. A package board having a core board on each surface of which a conductor layer is formed, and another conductor layer is formed on said conductor layer with an interlaminar resin insulating layer therebetween, and a conductor layer formed on the top of any of said interlaminar resin insulating layers is used as an electrode layer, wherein

the land of a via-hole formed through an interlaminar resin insulating layer formed on the bottom surface of said package board, disposed in a conductor layer formed as said electrode layer, is united with a pad connected to a via-hole formed through an interlaminar resin insulating layer formed on the top surface of said package board.

7. A package board comprising a multi-layer conductor circuit formed with each of a plurality of interlaminar resin insulating layers therebetween, a plurality of soldering bumps formed on the IC chip mounted side surface, as well as on the other surface connected to another board so that a space between the surface connected to another board and another board is sealed with resin, wherein

a soldering bump formed on the surface of said package board, connected to another board, is formed in a via-hole.

8. A package board comprising a multi-layer conductor circuit formed with each of a plurality of interlaminar resin insulating layers therebetween, a plurality of soldering bumps

formed both on the IC chip mounted side surface and on the other side surface connected to another board so that a space between said surface connected to another board and another board is sealed with resin, wherein

each of said soldering bumps formed on the surface of said package board, connected to another board, is formed on each of a plurality of via-holes.

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